REMARKS

To further demonstrate that the Applicants herein were in full possession of the claimed invention prior to the publication date of the Master '716 patent, Applicant's attorney reminds the Examiner of the following.

The inventor has already sworn he prepared the documents leading to the provisional application prior to September 26, 2002. The Master '716 patent publication was part of that provisional. Master '716 discloses the claim limitations as follows:

7. As per claim 1: Master '716 teach an integrated circuit comprising:
   a. A plurality of computational (¶45);
   b. A first and a second processing node each having a core processor with a common architecture (¶12; ¶47; ¶28) (Paragraph 12 shows that they have common architectures. Paragraph 47 shows that each matrix has a core. Paragraph 28 that either the KARC or MARC can constitute a first node.), wherein the common architecture is configurable in response to a first configuration command to be a control node adapted to control an interconnection of said computational elements to perform a selected task and configure in response to a second configuration command to be a programmable scalar node (PSN) adapted to perform a computational application (¶29);
   c. A first memory associated with said first processing node; a second memory associated with said second processing node (¶44; Figure 4) (Paragraph 44 shows that each mode has local memory. Figure 4 shows that the memory is associated with the core of the node.);
   d. A first interface for coupling said core processor of said first processing node to said first memory and to said computational elements (¶29; ¶45; ¶47; Figure 3, data interconnect network); and
   e. A second interface for coupling said core processor of said second processing node to said second memory and to said computational elements, the first interface and the second interface having the same architecture (¶25; ¶29; ¶45; ¶47) (Paragraph 25 shows that the MARC and KARC are made of the same matrices as the first processing node, and therefore will be set up the same way.).

8. While Master does not teach a data cache and instruction cache, the implementations and benefits of Harvard-architecture caching is extremely well known in the art. It would have been obvious to one of ordinary skill in the pertinent art to apply a Harvard caching system to Master.

9. As per claim 2: The integrated circuit of claim 1 further comprising means for temporally adapting said second node and said computational elements to perform a selected function (¶40).

10. As per claim 3: The integrated circuit of claim 2 wherein said temporal means further comprises executable code defining said selected function stored in at least a memory (¶40).

11. As per claim 7: The integrated circuit of claim 1 wherein said computational elements include a plurality of arithmetic nodes, a plurality of bit-manipulation nodes and a plurality of finite state machine nodes (¶45).

12. As per claim 8: The integrated circuit of claim 1 further comprising a plurality of said second processing nodes and an interconnection network, the plurality of said second processing nodes coupled through the interconnection network to said first processing node and plurality of computational elements (¶26; Figure 1).

13. As per claim 9: An integrated circuit comprising:

a. A first node having:

   i. A first core processor configurable in response to a first configuration signal into a controller node for execution of operating system code (¶26, ¶29);

   ii. A first memory for storing operating system executable code (¶44);

   iii. Means for transferring operating system executable code and data from said first memory to said first core processor (¶29); and

   iv. A plurality of computational elements adapted to perform a selected function (¶33);

b. A second node having:

i. A second core processor having the same circuit architecture as the list core processor, the second core processor configurable into a RISC processor for execution of application code (¶28);

ii. A second memory for storing application code (¶44);

iii. Means for transferring application code and data from said second memory to said second core processor (¶29); and

iv. An interconnection network coupling said controller node and said RiSC processor to said plurality of computational elements to perform the selected function (¶26) (Figure 1, item 1 10);

c. A first interface coupling said first core processor to said interconnection network (Figure 1, item 110) (Part of matrix interconnection network 11 0 connects the individual matrices into the network); and

d. A second interface coupling said second core processor to said interconnection network, the first and second interfaces having a common interface architecture (Figure 1, item 1 10) (Part of matrix interconnection network 1 10 connects the individual matrices into the network).

14. As per claim 14: An integrated circuit having a plurality of computational elements and an interconnection network for interconnecting said computational elements, said integrated circuit comprising:

a. A controller node comprising:

i. A first core processor for executing operating system code (¶47);

ii. A first memory for storing operating system executable code (¶44); and

iii. A first interface coupled to said first core processor and to the interconnect network, for receiving and transferring to the first core processor a portion of an input stream from an external source, said input stream having configuration information or executable code (¶29); and

b. A programmable scalar node comprising:

i. A second core processor for executing instructions, the second core processor having the same circuit architecture as the first core processor (¶28, ¶29);

ii. An instruction memory for storing said instructions (¶44);

iii. A data memory (¶44); and

iv. A second interface coupled to said second core processor and to the interconnection network for receiving an input stream from the controller node, said input stream having configuration information (¶29).

15. While Master does not teach a data cache and instruction cache, the implementations and benefits of Harvard-architecture caching is extremely well known in the art. It would have been obvious to one of ordinary skill in the pertinent art to apply a Harvard caching system to Master.

16. As per claim 15: Master et al. do not teach the integrated circuit of claim 14 further comprising means for accessing said first core processor and said first memory to debug error conditions. This would entail a JTAG controller, which is well known in the art along with its many known advantages, and it is obvious to see why Master et al. would have motivation to add it.

17. As per claim 16: The integrated circuit of claim 14 further comprising means for node-to-node communication (¶29).

18. As per claim 17: The integrated circuit of claim 14 further comprising a second memory for storing executable code for controlling the interconnection of said computation elements in response to configuration information (¶40).

19. As per claim 22: The integrated circuit of claim 14 further comprising means for controlling power consumption (Abstract).

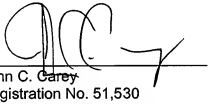
20. As per claim 23: The integrated circuit of claim 1, wherein the control node is configured to change the interconnecting of said computational elements and said first and second processing nodes to define a second task to achieve a second function previously not available or existent (¶41).

21. As per claim 24: While Master does not explicitly state that the PSN nodes (Figure 1, items 150EN) can be configured as RISC processors, such would have been inherent since the logic required to implement a RISC processor is present in the nodes (¶28) and RISC processors are well known to be able to perform various tasks which would be beneficial to Mater's system.

22. As per claim 25: The integrated circuit of claim 9, wherein the controller node is configured to change the interconnection network coupling said controller node to said computational elements to perform a second selected function not available or existent (¶41).

Therefore the inventors were in full possession of the claimed invention prior to its publication date. This affidavit as submitted was proper and met all the requirements of Rule 131. Therefore, the Master '716 publication must be withdrawn as a reference.

Respectfully submitted



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